January 1986

SUPER BOARD
MULTIPURPOSE INTERFACE
USER'S MANUAL

OS9 VERSION

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FIRST EDITION
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INTRODUCTION

The SUPER BOARD interface combines a number of functions usually found in individual plug-ins for the Radio Shack Color Computer. The board contains dual RS-232 Serial data ports with software controllable baud rates, a parallel printer port, and a battery-backed up real time clock. When used in conjunction with the OS9 operating system, the board allows the color computer to perform multi-tasking. The serial ports operate at RS-232 levels and support DTR, CTS, and DCD. Baud rates are adjustable from 300 to 19.2K. The parallel printer port allows for full Centronics compatible operation. The real time clock has features such as software selectable daylight savings time, automatic leap year compensation, 12/24 hour operation, and an alarm with audible output.

SECTION ONE

1.1 FEATURES

The SUPER_BOARD interface features include

a. Dual serial ports
   1. One driver (acia) for terminals modems and printers
   2 When logged on via a modem, when the carrier is dropped the driver will automatically generate an EOF logging the user off the system
   3 Very small software overhead for data transmission(hardware not software).
   4 Interupt driven so characters will be captured during disk access
   5 Support of data carrier detect(DCD) data terminal ready (DTR) and clear to send (CTS).

b. Parallel printer port
   1. Standard centronics parallel interface
   2. Very small software ovehead

c. Real time clock
   1.Automatic startup when booting OS9(stime) when stime is put into the startup file
   2. No time loss during floppy disk access as with software clock
   3. Automatic leapyear compensation
   4. Automatic seting of daylight saving time
   5. New "setime" program for enchanced features of hardware clock

INSTALLATION

2.1 UNPACKING INSTRUCTIONS

Unpack the SUPER_BOARD from the shipping carton(be sure to save the original carton as all returns must be in it) The following items should be present.

a. The SUPER_BOARD

b. Instruction manual

c. A floppy disk with the drivers

After verifying that all items ,including any additional or optional parts are present,inspect each item for shipping damage. Insure that there are no broken parts. If there is, please notify LR TECH as soon as possible

2.2 SYSTEM HOOKUP

a.The color computer must be off

b. The expansion interface must be off

c. Plug the SUPER_BOARD into slot 2 of the expansion interface(the 36 pin connector should be to your right).

e. Connect the parallel printer port to the printer

f. Connect the two serial ports to there respective devices(modems,terminals or a serial printer).

g. Apply power to the entire system

h. The sign on logo should now appear on your CRT, if not check steps a thru g.

NOTE: see cable wiring lists in section 2.5

2.3 SOFTWARE INSTALLATION

At this point OS9 should be booted up as normal and the distribution disk with the driver on it should be backed up(see commands manual pg.63). The disk should contain the following under the CMDS directory.

a. T1 & t2 device descriptors for terminals and modems #1 & #2

b. P1 & p2 device descriptors for serial printers #1 & #2

c. Term.super device descriptor for device /Term to allow booting up on a terminal

d. Acia the device driver for t1,t2,p1,p2 and term.super

e. P3 device descriptor for the original color computer serial printer port to be used with PRINTER

f. P the device descriptor for the parallel printer port

g. Pia the device driver for the parallel printer port

h. Clock a new clock module for reading the new hardware realtime clock and to allow multi tasking

i. Stime this file enables the real time clock and lets OS9 know that there is a clock module installed and ready. LI only

j. Setime a file to set the hardware clock

k. Bootlist a list of modules for OS9gen to create a new system disk.

l. Save.modules a procedure file to save the current in memory modules to disk.

m. Copycmds a procedure file to copy over the necessary commands to create a new system disk

At this point you will have to choose what descriptors and drivers will be placed in memory at boot time. There are however, some restrictions. They are as follows. Because there are not four serial ports, it makes no sense to load in t1 and p1 as they both share the same hardware port. This is also true of t2 and p2. If using the serial ports for remote terminals or modems, "clock" must be installed. The reason for this is that the SUPER_BOARD uses the FIRQ line through the expansion buss on the side of the color computer going through a PIA and not direct to the FIRQ line on the processor . The PIA, being an edge sensitive device and not level sensitive, can possibly hang up the serial ports.The way around this is to check the serial ports at every time slice and clear them if need be. To keep the serial drivers as small as possible, they can not be unlinked out of memory once installed, as they take over the FIRQ vector(if you modify the drivers BEWARE).

2.4 EXAMPLE SYSTEMS

The following are some of the possible system configurations.

SYSTEM A. If one remote terminal "t1" and two printers one serial and one parallel with th hardware realtime clock the bootlist should contain. acia,boot,ccdisk,ccio,clock,d0,d1,d2, init,ioman,p,pia,pipe,piper,pipeman,RBF,SCF,shell,sysgo,term,t1, p1.

SYSTEM B. If two remote terminals or modems(modems automatically log the user off if the carrier is droped)and a parallel printer the bootlist should contain the following.
acia,boot,ccdisk,ccio,clock,d0,d1,d2,init,ioman,p,pia,pipe,piper

SYSTEM C. If the system wanted to boot up to a dumb terminal from a hard disk and have another terminal for multi-user capability with a parallel printer port, the bootlist should be as follows acia,boot,hdisk,clock,h0,init,ioman,p,pia,pipe,piper

As can be seen there are many possible combinations. You may want to make several diffrent systems to suit different needs This can also free up quite a bit of memory, as much as 48k or more.

NOTE: There are no provisions for floppy disk time out when booted up to a terminal. They must be turned off by writting 00 to $FF40 or use a hard disk system only.

3.0 HARDWARE INSTALLATION

In order to use this board to it's fullest potential some cables will have to be made, two for the serial ports and one for the parallel printer port .

The serial port cables are a subminiture 25 pin male D type Positronic ind MD25M-200 or equivalent for jacketed cable or an AMP 206771-1 for ribbon cable.These connectors are industry standard cables used for RS232-C serial data transmission.

The parallel printer cable is a 36 pin Centronics compatiable connector such as an Amphenol 57-30360 or an Amp 552274-1 or equivalent type.

When looking at the SUPER_BOARD, t1/p1 is on the top right and t2/p2 is on the top left.

When using an auto answer modem the modem should not echo any status back to OS9. If the modem does echo any thing when a connect is made Tsmon, will get very confused.

See the following wire list for a particular type of installation:

CABLE WIRING DIAGRAMS

REMOTE TERMINAL CABLE

SUPER_BOARD t1 & t2			terminal
2	data out	-------->	3 data in
3	data in	<--------	2 data out
5	CTS	<-------	20 DTR
7	common	<------>	7 common
8	DCD	not used	
20	DTR	------->	5 CTS

MODEM CABLE

SUPER_BOARD			MODEM
2	data out	-------->	2 data in
3	data in	<-------	3 data out
5	CTS	<-------	5 CTS
7	common	--------	7 common
8	DCD	<-------	8 DCD out
20	DTR	------->	20 DTR in

NOTE: In order for the driver to generate an EOF when the carrier is dropped DCD must be connected.

SERIAL PRINTER CABLE

SUPER_BOARD		PRINTER
2 data out	------->	3 data in
3 data in	not used	
5 CTS	<-------	11 SSD (Busy)
7 common	--------	7 common
8 DCD	not used	
20 DTR	not used	
		¦---> 6 DSR
		¦
		¦---- 20 DTR

NOTE: for further information see your printer manual.

PARALLEL PRINTER CABLE

SUPER_BOARD		PRINTER
1 data strobe	-------->	1
2 data bit 1	-------->	2
3 data bit 2	-------->	3
4 data bit 3	-------->	4
5 data bit 4	-------->	5
6 data bit 5	-------->	6
7 data bit 6	-------->	7
8 data bit 7	-------->	8
9 data bit 8	-------->	9
10 acknowledge *	<-------	10
11 Busy	<-------	11
12 Fault	<-------	12
16,17,19,20,21,22,23 24,25,26,27,28,29,33	common	19 thru 30

NOTE: * Denotes active low signal.

SECTION FOUR

SOFTWARE DESCRIPTION

4.1 setime sets the hardware real time clock it's use is
setime <enter>

```
                yy/mm/dd hh:mm:ss
        Time    86 01 10 15 00 00
set for daylight savings time (Y/N) ? (answer Y or N) <enter>
```

NOTE: the real time clock in it's current configuration is setup to use a 24 hour time format and hour should be entered 00 thru 20. Two digits must be typed for each entry even if that entry is only one digit(use leading zero as in above example.

4.2 Xmode use xmode to change baud rates,word length and parity(see pg 117 of red commands manual).

BAUD RATE VALUE	ACTUAL BAUD RATE
0	300 baud
1	600 baud
2	1200 baud
3	2400 baud
4	4800 baud
5	9600 baud
6	19200 baud

TYPE = XX

01	--------> 7 bits even parity 2 stop bits
05	--------> 7 bits odd parity 2 stop bits
06	--------> 7 bits even parity 1 stop bit
07	--------> 7 bits odd parity 1 stop bit
11	--------> 8 bits no parity 2 stop bits
15	--------> 8 bits no parity 1 stop bit (see note)
16	--------> 8 bits even parity 1 stop bit
17	--------> 8 bits odd parity 1 stop bit

NOTE: this is the default device driver value as supplied.
this value can only be changed before the device is used and once used can't be changed unless done direct by debug.

4.3 stime this file is to be used at system startup and should be placed into the commands directory and should be called by the startup file as it starts up OS9's tick clock and enables the hardware real time clock.

HARDWARE DESCRIPTION

The Super Board contains address decoding for all onboard devices, so that the board can be used in any of the multi-pak slots. These devices are mapped as follows:

1. clock - hex FF70
2. Serial Port #1 - hex FF68
3. Serial Port #2 - hex FF6A
4. Parallel port - hex $FF64

Note: The RTC (real time clock) is a register oriented device and will be discused later.

1. Serial Data Ports

The Serial Ports each consist of an asyncoronous reciever-transmitter (U16,U17-6850), input buffers (U18,U20-1489), and output buffers (U19-1488). The 6850 contains two registers, a data register and a control register. The control register controls clock rates, byte size, parity, and interrrupt control. The data register provides the processor with the data received on the port and when written to it delivers the data from the processor buss to the output port. The buffers provide conversion from to and from RS-232 levels. Adjacent to the serial ports is the baud rate oscillator and associated switching circuit. The oscillator circuit provides seven baud rates - 300, 600, 1200, 2400, 4800, 9600, and 19.2k. These corespond to baud = 0 for 300 up to baud = 6 for 19.2k using xmode.

2. Real Time Clock

The real time clock is made up of the RTC chip (U7-6818), address decoding circuitry (U5-7408) (U4-7400), and power down circuit (U6-7705). The 6818 is continuously powered either by the system power or the two batteries BT1 and BT2. Switch over to battery backup is accomplished by the power down supervisor U6 which maintains a chip enable (low) to the RTC only when the system power is above 4.75 volts. This signal is inhibited by an output from U10 (6821) to prevent erroneous writes to the RTC. The RTC internally contains a number of registers which make up the clock, alarm, and control. It also has 50 bytes of ram which is battery backed up. This ram and all the other registers may only be accessed by writing the address register with the register location then reading the data register. The address register is located at $FF70 and the data register is located at $FF71. An audible output is also supplied. This can be used for alarm or even a keyboard bell.

The location of Registers are:

Address	Function
$00	seconds
$01	seconds alarm
$02	minutes
$03	minutes alarm
$04	hours
$05	hours alarm
$06	Day of the week
$07	Date of the month
$08	Month
$09	Year
$0A	Reg A
$0B	Reg B
$0C	Reg C
$0D	Reg D
$0E thru $3F	Ram

REG A	* UIP	* DV2	* DV1	* DV0	* RS3	* RS2	* RS1	* RS0 *

UIP - The update in progress (UIP) bit is a status flag that may be monitored by the program. When UIP is a "1" the update cycle is in progress or will soon begin. When UIP is a "0" the update cycle is not in progress and will not be for at least 244 us (for all time bases). This is detailed in table 6.
The time, calendar, and alarm information in RAM is fully available to the program when the UIP bit is zero - it is not in transition. The UIP bit is a read-only bit, and is not affected by Reset. Writing the SET bit in Register B to a "1" inhibit any update cycle and then clear the UIP status bit.

DV2,DV1,DV0 - Three bits are used to permit the program to select various conditions of the 22-stage divider chain. The divider selection bits identify which of the three time-base frequencies is in use. Table 4 shows that time bases of 4,194304 MHz, 1,048576 MHz, and 32,768 KHz may be used. The divider selection bits are also used to reset the divider chain. When the time/calendar is first initialized, the program may start the divider at the precise time stored in the RAM. When the divider reset is removed the first update cycle begins one-half second later. These three read/write bits are not affected by RESET. This should not be changed by the user as it set by software (setime).

RS3,RS2,RS1,RS0 - The four rate selection bits select one of 15 taps on the 22-stage divider, or disable the divider output. The tap selected may be used"to generate an output square wave (SQW pin) and/or a periodic interrupt. The program may do one of the following: 1)enable the interrupt with the PIE bit, 2)enable the SQW output pin with the SQWE bit, 3)enable both at the same time at the same rate, or 4)enable neither.

REG B	* SET * PIE * AIE * UIE * SQWE * DM * 24/12 * DSE *

SET - When the SET bit is a "0", the update cycle functions normally by advancing the counts once-per-second. When the SET bit is written to a "1", any update cycle in progress is aborted and the program may initialize the time and calendar bytes without an update occuring in the midst of initializing. SET is a read/write bit which is not modified by RESET or internal functions of the MC146818.

PIE - The periodic interrupt enable (PIE) bit is a read/write bit which allows the periodic-interrupt flag (PF) bit in Register C to cause the IRQ pin to be driven low. A program writes a "1" to the PIE bit in order to receive periodic interrupts at the rate specified by the RS3,RS2,RS1 and RS0 bits in Register A. A zero in PIE blocks IRQ from being initiated by a periodic interrupt, but the periodic flag (PF) bit is still set at the periodic rate. PIE is not modified by any internal MC146818 functions, but is cleared to "0" by a RESET.

AIE - The alarm interrupt enable (AIE) bit is a read/write bit which when set to a "1" permits the alarm flag (AF) bit in Register C to assert IRQ. An alarm interrupt occurs for each second that the three time bytes equal the three alarm bytes (including a "don't care" alarm code of binary 11XXXXXX). When the AIE bit is a "0", the AF bit does not initiate an IRQ signal. The RESET pin clears AIE to "0". The internal functions do not affect the AIE bit.

UIE - The UIE (update-ended interrupt enable) bit is a read/write bit which enables the update-end flag (UF) bit in Register C to assert IRQ. The Reset pin going low or the SET bit going high clears the UIE bit.

SQWE - When the square-wave enable (SQWE) bit is set to a"1" by the program, a square-wave signal at the frequency specified in the rate selection bits (RS3 to RS0) appears on the SQW pin. When the SQWE bit is set to a zero the SQW pin is held low. The state of SQWE is cleared by the RESET pin. SQWE is a read/write bit.

DM - The data mode (DM) bit indicates whether time and calendar updates are to use binary or BCD formats. The DM bit is written by the processor program and may be read by the program, but is not modified by any internal functions or RESET. A "1" in DM signifies binary data, while a "0" in DM specifies binary-coded-decimal (BCD) data.

24/12 - The 24/12 control bit establishes the format of the hours bytes as either the 24-hour mode (a "1") or the 12-hour mode (a"0"). This is a read/write bit, which is affected only by software.

DSE - The daylight savings enable (DSE) bit is a read/write bit which allows the program to enable two special updates (when DSE is a "1"). On the last Sunday in April the time increments from 1:59:59 AM to 3:00:00 AM. On the last Sunday in October when the time first reaches 1:59:59 AM it changes to 1:00:00 AM. These special updates do not occur when the DSE bit is a "0". DSE is not changed by any internal operations or reset.

REG C	*	IRQF	*	PF	*	AF	*	UF	*	0	*	0	*	0	*

IRQF - The interrupt request flag (IRQF) is set to a "1" when one or more of the following are true: PF=PIE= "1" AF=AIE= "1" UF=UIE= "1" i.e., IRQF = PF.PIE+AF.AIE+UF.UIE

Any time the IRQF bit is a "1", the IRQ pin is driven low. All flag bits are cleared after Register C is read by the program or when the RESET pin is low.

PF - The periodic interrupt flag (PF) is a read-only bit which is set to a "1" when a particular edge is detected on the selected tap of the divider chain. The RS3 to RS0 bits establish the periodic rate. PF is set to a "1" independent of the state of the PIE bit. PF being a "1" initiates an IRQ signal and sets the IRQF bit when PIE is also a "1". The PF bit is cleared by a RESET or a software read of Register C.

AF - A "1" in the AF (alarm interrupt flag) bit indicates that the current time has matched the alarm time. A "1" in the AF causes the IRQ pin to go low, and a "1" to appear in the IRQF bit, when the AIE bit also is a "1". A RESET or a read of Register C clears AF.

UF - The update-ended interrupt flag (UF) bit is set after each update cycle. When the UIE bit is a "1", the "1" in UF causes the IRQF bit to be a "1", asserting IRQ. UF is cleared by a Register C read or a RESET.

b3 TO b0 - The unused bits of Status Register 1 are read as "0's". They can not be written.

REG D	*	VRT	*	0	*	0	*	0	*	0	*	0	*	0	*

VRT - The valid RAM and time (VRT) bit indicates the condition of the contents of the RAM, provided the power sense (PS) pin is satisfactorily connected. A "0" appears in the VRT bit when the power-sense pin is low. The processor program can set the VRT bit when the time and calendar are initialized to indicate that the RAM and the time are valid. The VRT is a read only bit which is not modified by the RESET pin. The VRT bit can be set by reading Register D.

b6 TO b0 - The remaining bits of Register D are unused. They cannot be written, but are always read as "0's."

3. Parallel Printer Port

The parallel printer port consists of the PIA (U10-6821) and buffers (U11,U12-74LS244). The PIA is configured by software to send 8 bit data and handshake with the chosen printer.

6.1 SERIAL PORT

The possible problems with the serial port's can be as follows.

PROBLEM	SOLUTION
No data to terminal/printer	wrong baud rate,parity or number of stop bits U10 bad baud rate sel
	Cable's wired wrong
	U19 bad
No data out of only 1 of the two serial ports	serial port chip bad U16 for T1 or U17 for T2 U19 bad Baud rate generators bad U13,U14 for T1&T2 in tha order
Data transmitted but not recieved	U18 bad for T1 U20 for T2

6.2 PARALLEL PORT

PROBLEM	SOLUTION
No printing	Cable wired wrong U10 ,U11 or U12 bad
Printer over prints line	use XMODE to turn on line feeds

6.3 REAL TIME CLOCK

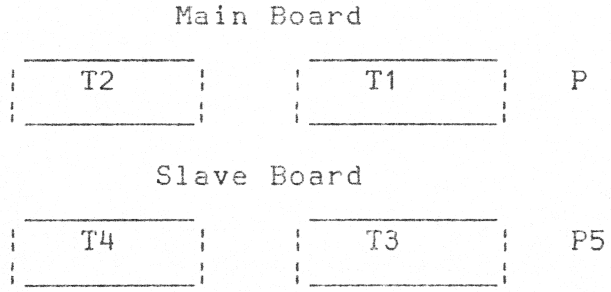
PROBLEM	SOLUTION
Clock does not keep time	Batteries low
Clock always has ERROR 246	stime not run Clock not enabled U4,U5,U6,U7 or U10 bad
Clock displays wrong time	Bad SAM chip in color computer Marginal timing cut Capacitors on E & Q lines in coco and expansion buss

SUPER BOARD
ADDENDUM LII

BOARD INSTALLATION

1. Open the Main super_board and remove the paper insulating the batteries.
2. Place the main Super_board in to slot #2
3. Place the slave board into slot #1
4. Build cables as per Super_board Manual

Port location



GENERATING A LEVEL II FLOPPY SYSTEM DISK

1. Format a disk for the new system
2. Place a backup of the Config disk into drive 1
3. Place a copy of the Super_Board driver disk into drive 0
4. Type chd /d0/LII <enter>
5 Type install.modules <enter>
6. Type chx /d1/cmds;chd /d1 <enter>
7. Place the freshly formatted disk into drive 0
8. Type config <enter> see level II manual for instructions.
   source drive is /d1
   destination drive is /d0
9. The modules that should be used are:
   - T1/P1 first terminal or serial printer on main board
   - T2/P2 second terminal or serial printer on main board
   - P parallel printer on main board
   - T3 3rd terminal on slave board
   - T4 4th terminal on slave board
   - P5 2nd parallel printer port on slave board
10. Place LR Tech disk back into /d1
11. Type chd /d1/LII <enter>
12. Type install.2 <enter>

13. The following step are if not using the 32 column screen
13a Type del /d0/startup <enter>
13b Type copy startup.levelii /d0/startup <enter>
13c Goto step 15

14. The following is for the 32 column screen
14a Type chd /d0 <enter>
14b Type edit startup <enter>
14c delete the line with setime on it
14d type Q to quit

15. Depress the reset push button twice
16. Type DOS <enter>
17. Type /d0/cmds/setime <enter>

GENERATING A LII HARD DISK SYSTEM DISK

1. Format a fresh 35 track single sided disk in /d0
2. Place the LR Tech disk into /d0
3. Type chd /d0/LII <enter>
4. Type Install.h0 <enter>
5. See step 9 above for module definitions
6. When system is generated be sure that the system disk has a CMDS directory with grfdrv in it or the system will not boot.

Note: this hard disk procedure file is setup for windows if the 32 column mode is desired copy back the original startup file and remove the line with setime in it

UTILITIES:

1. Beep — sounds the beeper for about 1 second
2. Unload — decrements the link count of a module to 0 this allows the port configuration to be changed. The steps are as follows:
   1. Type Unload T1 <enter>
   2. Type Deiniz T1 <enter>
   3. Type Deiniz T1 <enter>
   4. reconfigure T1 using Xmode
   5. Type Iniz T1 <enter>
   6. The port is now ready to use at a diffent setting.

BOOTING UP TO A TERMINAL

When booting up to a terminal grfdrv is no longer needed on the boot disk. Assemble the descriptor term.a in the SRC directory this is a copy of T1 renamed do not include T1 in the boot file. Include T2, T3, T4, P, P5, Pia, Acia, and Clock.
The mininum system files are as follows:

1. Os9p2
2. Ioman
3. CC3go
4. RBF
5. CC3disk
6. D0
7. D1
8. SCF
9. DD